IN THE CLAIMS

Please amend the claims as follows.

Please cancel claims 10-16, 25-29 and 33 without prejudice or waiver of patentable content.

1-16 (Canceled)

17. (Previously Presented) A transistor formed in a semiconductor substrate, the substrate including a surface and a region doped with an impurity which promotes one of either holes or electrons as a first majority carrier, the transistor comprising:

a collector region having an impurity therein which promotes the other of holes or electrons as a second majority carrier, the collector region extending from the surface of the substrate;

a base region having an impurity therein which promotes the first majority carrier, the base region comprising an intrinsic base region and a surrounding extrinsic base region, the intrinsic base region extending from the surface of the substrate into contact with a portion of the collector region;

an emitter region on the base region, the emitter region having a surface area smaller than a surface area of the intrinsic base region;

a first implant region interposed between the collector region and the base region, the implant region having an increased doping of an implant impurity and having an effective surface area greater than the surface area of the emitter region contiguous to the base region and less than the area of the intrinsic base region contiguous to the collector region; and

a second implant region formed in the collector region.

18. (Previously Presented) The transistor of claim 17, wherein the second implant region is formed at about the same level from the surface of the substrate as the first implant.

19. (Previously Presented) The transistor of claim 17, wherein the collector region includes a plug extending from the surface of the substrate, the plug being separate from the base region.

20. (Previously Presented) The transistor of claim 19, wherein the second implant region is formed in the plug at about the same level from the surface of the substrate as the first implant region.

21. (Previously Presented) The transistor of claim 17, wherein the transistor is an NPN transistor and the implant impurity in the first and second implant regions is phosphorous.

22. (Previously Presented) The transistor of claim 17, wherein the transistor is a PNP transistor and the implant impurity in the first and second implant regions is boron.

23. (Previously Presented) The transistor of claim 17, wherein the effective surface area of the first implant region minimizes carrier injection from the emitter region to the collector region outside the first implant region at high current operation of the transistor.

24. (Previously Presented) The transistor of claim 17, wherein the second implant region has a surface area greater then the area of an opening through which the second implant region is formed.

25-33. (Canceled)

34. (Previously Presented) A transistor, comprising:

an emitter having an emitter surface area;

a base having a base surface area with a lightly doped intrinsic base region and a more heavily doped extrinsic base region, wherein the emitter surface area is in contact with the base;

a collector in contact with the base;

a collector plug in the collector;

a first implant region intermediate the base and the collector, the first implant region having an implant surface area in contact with the intrinsic base, the implant surface area being greater than the emitter surface area and less than the intrinsic base surface area; and

a second implant region in the collector plug.

35. (Previously Presented) The transistor of claim 34, wherein the first implant region and the second implant region are positioned at a same depth.

36. (Previously Presented) The transistor of claim 34, wherein the first implant region and the second implant region are simultaneously formed by an angled implant such that areas of the first implant region and the second implant region are greater than areas of the openings through which the first implant region and the second implant region are formed.

37. (Previously Presented) The transistor of claim 34, wherein the first implant region and the second implant region are doped by a same source.

38. (Previously Presented) A transistor, comprising:

an emitter having a periphery and a lateral extent;

a base having a first portion and a second portion, the second portion having a lateral extent in contact with the emitter to define an emitter-base surface;

a collector in contact with the base; and

means for minimizing carrier injection from the periphery of the emitter region to the collector region at high current operation of the transistor, wherein the means includes a region in contact with the collector and the second portion of the base, the region including a first surface in contact with the second portion of the base and not in contact with the first portion of the base and a second surface in contact with the collector, the first surface having a larger lateral extent than the emitter-base surface, and a smaller lateral extent than the second portion of the base.

39. (Canceled)

40. (Previously Presented) A transistor, comprising:

an emitter;

a base having a first portion and a second portion, the second portion in contact with the emitter to define an emitter-base surface;

a collector in contact with the base to define a horizontal base-collector surface; and

means for minimizing base-collector capacitance and maximizing high current operation, wherein the means includes a region in contact with the collector and the second portion of the base, the region including a first surface in contact with the second portion of the base and not in contact with the first portion of the base and a second surface in contact with the collector, the first surface being larger than the emitter-base surface and smaller than the second portion of the base-collector surface.

41. (Canceled)